What is claimed is:

1. A memory array comprising:

a storage unit having a number of sections, each section having a number of word lines for accessing a line of memory in the storage unit;

decoders coupled to respective ones of the sections, such a decoder being operable to decode an N-bit address signal and responsively assert a signal on one of the word lines selected by the address signal; and

local clock buffers coupled to respective ones of the decoders, such a local clock buffer being operable to receive a clock signal and an address signal including M most-significant bits of the N-bit address signal and to generate a timing signal, wherein each of the decoders receives the timing signal from its respective local clock buffer and each decoder is operable to precharge responsive to a first phase of the timing signal and to evaluate the N-bit address signal responsive to a second phase of the timing signal, and wherein the local clock buffer is operable, responsive to a state of the M bits of the address signal, for selecting between holding its timing signal in a deasserted state and enabling its timing signal to follow the clock signal.

2. The memory array of claim 1, wherein the local clock buffers are static circuitry.

3. The memory array of claim 1, wherein the local clock buffers are operable to receive a valid-bit signal.

4. The memory array of claim 1, the storage unit having multiple ports, wherein each of the word lines is coupled to a number of decoders.

5. The memory array of claim 1, wherein the word lines are for read accesses to the storage unit.

6. The memory array of claim 1, wherein the word lines are for write accesses to the storage unit.

7. A method for a memory array, wherein the memory array has a storage unit with a number of sections and a number of decoders coupled by word lines to respective ones of the sections, and wherein each decoder is coupled to an associated local clock buffer, the method comprising the steps of:

a) receiving, by the local clock buffers, a clock signal and an address signal including M most-significant bits of the N-bit address signal; and

b) generating respective timing signals by the local clock buffers, wherein generating the timing signal by such a local clock buffer includes the steps of:

evaluating a state of the M bits of the address signal; and

selecting between holding such a timing signal in a deasserted state and enabling the timing signal to follow the clock signal responsive to the state of the M bits of the address signal;

c) receiving the timing signals from the local clock buffers by the respective decoders;

d) holding a precharging state by a number of the decoders responsive to the decoders's local clock buffers holding their respective timing signals in a deasserted state; and

e) evaluating the N-bit address signal and responsively asserting a signal on a selected one of the word lines by one of the decoders responsive to the decoder's local clock buffer timing signal following the clock signal.

8. The method of claim 7, wherein the evaluating of the state of the M bits of the address signal by the local clock buffers is continuous rather than being interrupted by a precharging state responsive to a clock signal.

9. The method of claim 7, comprising the step of the local clock buffers receiving a valid-bit signal.

10. The method of claim 7, the storage unit having multiple ports, wherein each of the word lines is coupled to a number of decoders.

11. The method of claim 7, comprising the step of accessing a line of memory in the storage unit associated with the selected word line, wherein the accessing is a read access.

12. The method of claim 7, comprising the step of accessing a line of memory in the storage unit associated with the selected word line, wherein the accessing is a write access.

13. A memory array comprising:

a storage unit having a number of sections, each section having a number of word lines for accessing a line of memory in the storage unit;

storage unit decoders coupled to respective ones of the sections, such a storage unit decoder being operable to decode an N-bit address signal and responsively assert a signal on one of the word lines selected by the address signal; and

local clock buffers coupled to respective ones of the storage unit decoders, wherein such a local clock buffer includes:

a number L of series-connected inverters, with the first of the L inverters operable for receiving a clock signal and the last of the L inverters operable to responsively output a timing signal;

a local clock buffer decoder for receiving a valid-bit signal and M most-significant bits of the N-bit address signal, wherein a decode logic function of the respective decoders varies depending upon the local clock buffer;

a control node, wherein an output of the local clock buffer decoder is coupled to the control node;

a pull-up transistor coupled, by conducting electrodes, between a voltage supply and an output of one of the L inverters, the pull-up transistor having a gate coupled to the control node so that if the control node is high the pull-up transistor tends to be turned off, and if the control node is low the pull-up transistor tends to be turned on; and

a isolation transistor having a gate coupled to the control node and having conducting electrodes interposed between ground and a transistor of a penultimate

one of the L inverters, so that if the control node is low this tends to isolate an output of the penultimate inverter from ground, permitting the pull-up transistor to pull up an output of the penultimate inverter, which in turn tends to drive the timing signal low, and if the control node is high this permits the timing signal to follow the clock signal;

wherein each of the storage unit decoders receives the timing signal from its respective local clock buffer and each storage unit decoder is operable to precharge responsive to a first phase of the timing signal and to evaluate the N-bit address signal responsive to a second phase of the timing signal.

14. The memory array of claim 13, wherein the local clock buffer decoder is coupled to the control node via an intermediate inverter.

15. The memory array of claim 14, wherein an electrode of a transistor of the intermediate inverter is coupled to ground by means of a control transistor, the gate of the control transistor being operable to receive a power save enable signal, and the local clock buffer includes:

a second pull-up transistor coupled, by conducting electrodes, between the control node and the voltage supply and having a gate for receiving the power save enable signal, so that if the power save enable signal is deasserted the second pull-up transistor tends to turn on and pull up the control node.

16. The memory array of claim 15, wherein an electrode of a transistor of the first one of the L inverters is coupled to ground by means of a second control transistor, and the local clock buffer includes:

control circuitry coupled between the first and second ones of the L inverters and coupled to a gate of the second control transistor.

17. The memory array of claim 1, wherein the local clock buffer decoders are operable to receive a valid-bit signal.

18. The memory array of claim 1, the storage unit having multiple ports, wherein each of the word lines is coupled to a number of storage unit decoders.

19. The memory array of claim 1, wherein the word lines are for read accesses to the storage unit.

20. The memory array of claim 1, wherein the word lines are for write accesses to the storage unit.